40610-600 ORDER WIRE, ISSUE 02

SYSTEM DESCRIPTION

1. REFERENCES

0406-4600 Wiring Diagram
41670 Telephone Interface
41632 DTMF Address Decoder
41620 Power Supply (Optional)

2. OPERATION

2.1. CALL ORIGINATION

A call is initiated by going off hook with the telephone handset and selecting the address code of the station to be called with the telephone touch-tone keypad. DTMF signaling tones are transmitted to all stations, with the called station detecting its address and ringing its telephone. The called station provides ringback to the initiating station until the call is answered or the ring time (typically 19 seconds) times out.

2.2. RECEIVING A CALL

When a station detects its DTMF address code, ring voltage is routed to the telephone. When the telephone handset is taken off hook, the ringing will cease and the conversation may proceed. The period of time the telephone will ring (ring time) is fixed by straps on the 41632 DTMF Address Decoder module. The ring time is typically set for 19 seconds at the factory, unless the customer requests otherwise. Refer to the 41632 module section of the manual for more detailed information.

3. DESCRIPTION

3.1. The 40610-600 Telephone Interface system provides an interface between a 4-wire transmission medium and a 2-wire or 4-wire telephone instrument. The system operates on a party line basis and provides selective calling via standard DTMF tones. The 4-wire port is 600Ω balanced and levels from +7 to -16 dBm can be accommodated in both the receive and transmit direction. Relay contact closures are provided for an M-Lead (off-hook) indication and an E-Lead (closed during ringing cycle).

3.2. The 41620-01 Power Supply module accepts -24 to -56VDC and provides a regulated -20VDC to the 41670 Telephone Interface and 41632 DTMF Address Decoder modules. If a well regulated -20 to -24VDC source is available, the 41620-01 Power Supply may be deleted and the source used to power the 41670 and 41632 modules directly. An external AC to DC converter is used when the power source is 95 to 250 VAC.

3.3. The 41670 Telephone Interface module supplies talk battery to the telephone instrument to power the microphone and DTMF generator. Ringback, off hook, and ring control for the on-board ring generator are included on the 41670 module. The 41670 module is strappable for operation with either a 4-wire or 2-wire telephone instrument.

3.4. The 41632 DTMF Address Decoder module bridges the Auxiliary Output of the Telephone Interface and provides the detection and address decoding of the DTMF signals. The 41632 module may be programmed for a one, two, three, or four digit address (strappable). Rocker switches are used to program the address code. Ring time is typically set for 19 seconds (strappable).

4. SIGNAL FLOW

4.1. TRANSMIT PATH

4.1.1. Signals present at the MIC input (pins U and V) of the 41670 Telephone Interface module are routed to the XMT port (pins H and J) when the telephone handset is off hook. Potentiometer R2 provides level adjustment for the transmit path. When the telephone handset is on hook relay K1 opens the transmit path to prevent spurious signals from being transmitted.

4.2. RECEIVE PATH

4.2.1. Signals present at the RCV port (Pins Y and Z) are routed through the 41670 module to the 2W port (pins U and V) for 2-Wire telephone applications, or to the 4-Wire RCVR output (pins P and R) for 4-Wire telephone applications. The Auxiliary Output (pins 21 and 22) is routed to the input of the 41632 DTMF Address Decoder. Potentiometer R3 provides level adjustment for the receive path.

5. INSTALLATION

5.1.1. Refer to Table B and wiring diagram 0406-4600 for required rear panel terminal block connections for system operation.

Extra caution must be exercised when connecting the power source to the system when the 41620 Power Supply is not used. The power source must provide a well regulated -20 to -24VDC for satisfactory system operation and prevent damage to the 41632 and 41670 modules.

6. ALIGNMENT

6.1. Alignment of the system has been performed at the factory. After installation the levels should be verified and adjusted as required. Attachment A lists the levels and impedances for the system. The telephone that will be used with the system should be connected to the system during the alignment process.

When a signal generator is connected to a test point, the port may be double terminated, causing a reduced signal level. To assure the correct level, bridge the test point with an AC voltmeter and set the signal generator level according to the AC voltmeter reading.

When taking output level readings, the AC voltmeter will be either terminated or bridged. If it is unknown which is correct, compare the two readings. If a 3.5 dB difference is noted, the bridged reading is correct. If a 6 dB difference is noted, the terminated reading is correct.

6.2. POWER

6.2.1. Connect a DC voltmeter to the TP1 and GND test points on the 41620 Power Supply. Turn power ON and read -20.0VDC. Adjust R15 on the 41620 module, if required.

6.3. TRANSMIT LEVEL

6.3.1. Turn system power OFF. Remove the 41670 Telephone Interface module and insert an Extender Card in its place. Insert the 41670 Telephone Interface module into the Extender Card. Turn power ON. Go off hook with the telephone handset.

6.3.2. Connect a "floating" (earth ground isolated at the AC supply) signal generator to pins U and V on the Extender Card (the signal ground side of the signal generator must be isolated from the talk battery circuitry by a 2μf capacitor). Set the signal generator frequency to 1 KHz at the level specified by Attachment A for the Telset MIC.

6.3.3. Connect the AC voltmeter (terminate if required) to pins H and J on the Extender Card. Read the level specified by Attachment A for XMT port. Adjust R2 on the 41670 module, if required. Go on hook with the telephone handset and verify the 1 KHz tone is not present on the AC voltmeter.

6.4. RECEIVE PATH

6.4.1. Connect a signal generator (not "floating") to pins Y and Z on the Extender Card. Set the signal generator frequency to 1 KHz at the level specified by Attachment A for the RCV port. Go off hook with the telephone.

6.4.2. 2 WIRE TELEPHONE ONLY

Connect a "floating" AC voltmeter (earth ground isolated at the AC supply) to pins U and V. The signal ground side of the AC voltmeter must be isolated from loop current by 2 μf capacitor. Go off hook. Read the level specified by Attachment A for the Telset RCVR. Adjust R3 on the 41670 module, if required.

4 WIRE TELEPHONE ONLY

Connect a "floating" AC voltmeter (earth ground isolated at the AC supply) to pins P and R. Read the level specified by Attachment A for the Telset RCVR. Adjust R3 on the 41670 module, if required.

6.5. Hybrid Balance (2 Wire telephone only)

6.5.1. The signal generator should be connected as described in step 6.4.1. and the telephone should be off hook.

6.5.2. Connect the AC voltmeter (not "floating") to pins H and J. Terminate the AC voltmeter if required. Adjust R1 on the 41670 module for a minimum reading on the AC voltmeter. The minimum reading obtained should be greater than 16 dB below the level specified by Attachment A for the XMT port.

6.6. RING TRIP ADJUSTMENT

CAUTION:
Do not touch the circuitry of the Telephone Interface or the Extender Card while the ring generator is active. The ringing voltage is hazardous and may cause injury.

6.6.1. Go on hook with the telephone handset. Enable the ring generator by connecting a clip lead between pin B and pin M on the Extender Card. The telephone should ring with a steady on/off duty cycle.

6.6.2. Go off hook with the telephone while it is ringing and verify that the ringing stops immediately. There is no adjustment for the ring trip level.

Turn power OFF. Remove the Extender Card and 41670 module.
Re-install the 41670 module in the system.

41620 REGULATED POWER SUPPLY

UNIT DESCRIPTION, ISSUE 08 P3

1. REFERENCES

1416-1202 Regulated Power Supply Schematic

2. GENERAL

The Raven 41620 Regulated Power Supply provides a regulated -20 Volt DC (@ 1.2A max.) output from an unregulated supply.

The 41620 has two input power options available. The 41620-01 regulates an input voltage ranging from -24 to –56 VDC. The 41620-02 provides a regulated output from either a 110 VAC or a 220VAC (50/60Hz) source.

The 41620 provides foldback current limiting at an output current of approximately 1.2 amperes. The 41620 can be modified at the factory to increase the maximum output current if required. Included on the 41620 is an ON/OFF power switch and a fuse in series with the input. The output is factory set at –20 VDC but is adjustable from –18 VDC to –24 VDC.

3. SPECIFICATIONS

Input Voltage	
Option -01	-24 VDC TO –56 VDC
Option -02	110 VAC or 220 VAC (50/60 Hz)
Output Voltage	-20 VDC regulated -18 VDC to –24 VDC adjustment range
Output Current	1 ampere @ -20 VDC foldback current limiting occurs @ approximately 1.2A
Output Voltage Ripple	≤ 75 mv (full load)

4. THEORY OF OPERATION

Power input to the 41620 is derived from either a -24 to –56 VDC source in the 41620-01 version or from a 110VAC or 220VAC 50/60Hz source in the 41620-02 version.

4.1. 41620-01 DC OPTION

The DC input voltage is applied between pins R, S, (optionally pin D or pin N) and Ground (pin B) through CR8, fuse F1, power switch S1 and the "DC" strap. The input voltage is then applied to the emitter of the series pass transistor Q1 via R9.

4.2. 41620-02 AC OPTION

The AC input is applied to pins U and W with the external ground connected to pin Y or Z. The input voltage completes the circuit through "AC" strap, fuse F1 and power switch S1 to the primary of transformer T1. T1 steps down the incoming 110 VAC or 220 VAC to a nominal 32 VAC.

The 32 VAC is full wave rectified by the silicon bridge rectifier CR1. Capacitor C1 helps eliminate the ripple component on the unregulated DC. The unregulated DC is applied to the emitter of the series pass transistor Q1 via R9.

4.3. DC REGULATOR

U1 is a 723 Integrated Circuit voltage regulator which provides a regulated output to the base of transistor Q2. Q2 provides the current drive to the base of the series pass transistor Q1.

Resistors R11 and R12 form a voltage divider that is referenced to the –20 V regulated output and driven by the "Voltage Reference Output" of the 723. This combination provides a voltage that is fixed in reference to the –20 V regulated output. This voltage drives the "Inverting Input" of the 723. The voltage for the "Non-inverting Input" of the 723 is determined by the setting of R15 in combination with R13 and R14. R15 is used to adjust the –20 V regulated output, which can be monitored at TP1. Both R15 and TP1 are near the switch at the front of the board for easy access.

4.4. FOLDBACK CIRCUITRY

R9, R1, R2, and Q4 comprise a current sensing circuit and determine when foldback occurs. R5 and R6 provide a reference voltage to the inverting input of comparator U2.

A –16 VDC supply is derived from the input voltage via R8, CR2, and C3 to power comparator U2. R3, R4, and CR4 provide a secondary reference voltage to the inverting input of comparator U2. These components insure control over the foldback circuitry even when the regulated output voltage drops to 0.

When the output current exceeds 1.2A, transistor Q4 will turn on, causing the output of comparator U2 to switch. This turns transistor Q3 on which turns transistor Q2 off and limits current flow through the series pass transistor Q1. Diode CR5 protects the output of the 723 regulator when foldback occurs.

4.5. CR7 is a "Power On" LED indicator. This LED will be illuminated when the 41620 is turned ON and the regulated output voltage is present.

41632 DTMF ADDRESS DECODER

UNIT DESCRIPTION, ISSUE 08 P1

1. REFERENCES

1416-1320 DTMF Address Decoder Schematic

2. GENERAL

2.1. The Raven 41632 DTMF Address Decoder provides 2 of 7 or 2 of 8 DTMF tone detection for one, two, three, or four digit addressing. For call decoding, digit selection is performed by setting DIP switches (up to four) to respond to the desired digits. A strap selectable interdigit timeout sets the allowable delay time between correct digits. To prevent loading of the receive line, the input to the 41632 module is a balanced high impedance input.

2.2. Two Correct Address outputs are provided. One Correct Address output resets after a strap selectable time period (interdigit/ring-time timeout) or an external reset ("*" or "#"). The second Correct Address output can only be reset by an external reset, or optionally, the DTMF ALL CLEAR (#).

2.3. The DTMF ALL CLEAR (#) and ALL CALL (*) tone pairs have outputs provided. The ALL CALL can be used in two ways. (1) Selecting an ALL CALL tone pair for more than one second allows the ALL CALL output to go active for the duration of the tone. (2) Selecting an ALL CALL tone pair for less than one second allows the ALL CALL (*) tone to be a generic digit. This allows for group call capabilities (i.e. addresses 121, 122, 123, and 124 would be considered correct addresses when the 41632 module receives the tone sequence 1-2-*).

3. SPECIFICATIONS

Power	-20VDC @ 50mA max.
Environmental	
Operating Temperature	0° to 50°C
Storage Temperature	-20° to +85°C
Relative Humidity	0 to 95%, non-condensing
Signal Input	
Impedance	100KΩ @ 1KHz
DTMF Detect Level	-25dBm minimum to +6dBm maximum
Minimum Tone Duration	40mSec.
Signal-to-Noise Ratio	12dB minimum
Reset Input	Active Ground
DTMF Tones	
Detector Bandwidth	± 1.5%
Allowable Twist	± 10dB
Inter-digit pause detect time	40mSec.
Signal Level Range	-23 to +7dBm

Timers	
Inter-Digit Timeout and Ringtime	Minimum = 4.7 seconds Maximum = 1 min. 15 sec.
Timed Correct Address Delay	Minimum = 37 mSec. Maximum = 2.4 seconds
Wrong Digit Holdoff	Minimum = .25 seconds Maximum = 19 seconds
Outputs	
ALL CALL, ALL CLEAR, Correct Address 1 & 2	Open Collector, ground when active
Wrong Digit	Open Collector, -20V when active
Logic "1"	Ground
Logic "0"	-5VDC

4. ADDRESS DIGIT PROGRAMMING

The 41632 DTMF Address Decoder detects and utilizes Dual Tone Multi-frequency (DTMF) signals to provide selective address decoding functions. DTMF signals are unique tone pairs generated by standard Touch Tone encoder arrays. Each button on a Touch Tone encoder is identified by the pair of frequencies generated when the button is pushed. Four low-group frequencies correspond to the four rows of buttons, and four high-group frequencies correspond to the four columns. The fourth column (1633Hz) is typically used only in special control applications.

1	2	3	A	697Hz	
4	5	6	B	770Hz	
7	8	9	C	852Hz	LOW GROUP
*	0	#	D	941Hz	
1209Hz	1336Hz	1477Hz	1633Hz		

HIGH GROUP

To program the 41632 DTMF Address Decoder, determine the number of digits to be used (one, two, three, or four) and install the appropriate strap (CA 2) or set the switch SW5 (CA 1):

	Correct Address 1	Correct Address 2
One digit Code:	SW5 switch 1	CA 2 DIGIT 1
Two digit Code:	SW5 switch 2	CA 2 DIGIT 2
Three digit Code:	SW5 switch 3	CA 2 DIGIT 3
Four digit Code:	SW5 switch 4	CA 2 DIGIT 4

Four DIP switches labeled SW1 (1st Digit), SW2 (2nd Digit), SW3 (3rd Digit) and SW4 (4th Digit) are the correct address programming switches. The 4 individual switch positions on each switch correspond to the code from the DTMF tone detector U4. Refer to the table below for digit programming information.

0 = off; 1 = on

DTMF	Switch Position				DTMF	Switch Position			
Digit	1	2	3	4	Digit	1	2	3	4
1	1	0	0	0	9	1	0	0	1
2	0	1	0	0	0	0	1	0	1
3	1	1	0	0	*	1	1	0	1
4	0	0	1	0	#	0	0	1	1
5	1	0	1	0	A	1	0	1	1
6	0	1	1	0	B	0	1	1	1
7	1	1	1	0	C	1	1	1	1
8	0	0	0	1	D	0	0	0	0

For example, if the address code of 357 is to be detected, either SW5 switch 3 is selected and/or CA 2 DIGIT 3 is installed. Set the switches on SW1 to correspond to the DTMF digit 3 (1100). Set the switches on SW2 to the DTMF digit 5 (1010). SW3 will be set to correspond to the DTMF digit 7 (1110). SW4 can be set to anything as its setting is ignored in this example.

5. THEORY OF OPERATION

5.1. DTMF Tone Detection

The input signal enters the 41632 module on pins D and E and is routed to the input buffer U3A-U3C. Input buffer U3 is high impedance and converts the signal to a single ended format. The signal is then routed to the input of the DTMF detector (U4). U4 detects the DTMF tones. When a valid DTMF tone pair is detected, U4 brings its strobe (pin 15) high, and sets its data lines (Q0, Q1, Q2, and Q3) to the corresponding DTMF tone pair.

5.2. TIMING FUNCTIONS

U2 is a binary ripple counter with an R-C oscillator on its input. The output of U2 (pin 1) is approximately 27Hz, and connects to another binary ripple counter (U1). U1 divides the 27Hz clock in binary steps and provides the resultant frequencies to its Q outputs. The frequencies are used to create the interdigit timeout/ring time, and the enable delay. When the 41632 is in the idle state, U1 is continuously being clocked and stepping through its Q outputs. When a correct digit is detected, U1 is reset to zero to initialize the timing sequence.

The ENABLE DELAY straps are used to enable the Correct Address 1 output (pin F). The INTERDIGIT TIMEOUT/RINGTIME straps provide two functions. The first function is used to set the timeout between valid digits. The second function is used to set the time the Correct Address 1 (pin F) remains active. Only one strap is installed for the interdigit/ringtime. For example, if an interdigit timeout is strapped for 4.7 seconds, then the correct address 1 output (pin F) will remain active for 4.7 seconds.

5.3. ADDRESS DETECTION

DIP switches SW1, SW2, SW3 and SW4 are used to select the digits to be recognized as the correct address. SW1 selects the first digit, SW2 selects the second digit, SW3 selects the third digit, and SW4 selects the fourth digit. The four positions on the switch correspond to the DTMF code. Refer to section 4 of this description for specific information on correct address programming.

Octal counter (U12) provides a sequencing logic high (ground) on one of its eight Q outputs, five of which are used. When U12 is reset, either from an interdigit timeout, wrong digit, or an external reset (pin R), its Q0 output (pin 2) is at logic high. Output Q0 enables U11, a four bit selector via U8A, and selects the data present on its X inputs (SW1). This data is presented at Exclusive NOR gate U9.

When a DTMF digit is detected, U4 brings its strobe active (high), enabling U18, sections A, B, C, and D, and places the DTMF code on its data outputs. These data outputs connect to the Exclusive NOR, U9.

If the data from U7 or U11 (SW data) and U4 (DTMF tone received data) agree, then the DTMF tone is a correct digit. All outputs of U9 are high causing the output of U13A to go high. The output of U13A connects to AND gate U18A, through diode CR2. The output of U18A connects to the CLOCK input of U12. When the correct digit is detected, U18A output goes low. When the tone ends, U18A goes high, causing U12 to clock to Q1, and U1 to reset. If the CA 2 DIGIT 1 strap is installed, U17B is set, causing transistor Q4 to turn on (pin N, CORRECT ADDRESS LATCHED). Likewise, if the CA 1 SW5 switch 1 is ON, the data input of U17A is set high. As the output of U1 (ENABLE DELAY strap)

goes high, the data is latched into U17A, causing Q1 to turn on (pin F, CORRECT ADDRESS 1). For each correct digit detected, U12 is clocked, enabling the different switches (SW5 switch 2, 3, and 4).

If the data from U7 or U11 (SW data) and U4 (DTMF tone received data) disagree, then the DTMF tone is a wrong digit. If any output of U9 is low, it will cause the output of U13A to stay low. When the wrong digit is detected, U18A output stays high. The output of U18A connects to U18B. The output of U18B goes through time delay R16 and C25, and is inverted by U14C. The output of U14C clocks a high into latch U16A. The output of this latch enables counter U6. During the strap selected wrong digit hold-off period the correct address digit counter U12 and the timed correct address latch (U17A) are held reset. If another DTMF strobe is detected during the hold-off period, the counter will be reset and the hold-off period starts over. When the counter reaches the strap selected time period the latch U16A is reset and the correct address digit counter and the timed correct address latch are enabled. The latch U16A can also be cleared by an "ALL CLEAR" or "RESET" condition which will reset & disable the counter U6.

The wrong digit function is disabled while Q1 is on (pin F, CORRECT ADDRESS 1) by the path through CR9 and ST6 to correct address latch (U17A) pin 1. This prevents turning off correct address if another DTMF key is pressed. To defeat this feature remove strap ST6.

The wrong digit hold-off signal is OR'd with the "RESET" signal so that U12 and U17A are also reset by a "RESET" condition.

5.4. The ALL CLEAR (#) tone pair has an open collector output. When the ALL CLEAR tone is detected, U18D goes low, turning on transistor Q2 (pin K ALL CLEAR). U15A also resets the wrong digit holdoff timer, U6.

5.5. The ALL CALL (*) tone pair has two functions. (1) If the ALL CALL tone pair is present for less than 1 second, then the tone is considered a correct digit if the Group Call option -02 is installed. When the ALL CALL tone is detected, U10A goes high. The output of U10A connects to U18A through diode CR3. The procedure occurs the same as a correct digit as described above. (2) If the ALL CALL tone pair is present for more than 1 second, U19B times out enabling U20C. The output of U20C goes low, turning on transistor Q3 (pin L ALL CALL). When the ALL CALL tone goes off, U20A goes high, resetting U12 and U17B.

5.6. ALL CLEAR RESET OPTION -01

If the ALL CLEAR reset option is installed, the 41632 will reset the interdigit timer (U12), the Correct Address 2 output (pin N), the Correct Address 1 output (pin F), the wrong digit latch U16A, and the wrong digit hold-off timer U6 upon the receipt of the DTMF digit ALL CLEAR.

5.7. GROUP CALL OPTION -02

This allows the caller to contact more than one Order Wire at the same time by using a (*) as a "wild card". For instance, by dialing 12**, all 4 digit phone numbers with 12 as their first two digits would ring.

41670 TELEPHONE INTERFACE MODULE
UNIT DESCRIPTION, ISSUE 12 P1

1. REFERENCES

1416-1706 Telephone Interface Schematic
1416-8706 Telephone Interface Block Diagram

2. GENERAL DESCRIPTION

The Raven 41670 Telephone Interface module provides the interface between a 4-wire port and touch tone Telset. The 41670 module can interface to either a 2-wire or 4-wire phone. The levels of the transmit and receive paths of the 4-wire port are each adjustable over a 23 dB range. Loop current circuitry provides talk battery to the Telset. A single set of Form C contacts are provided for M-Lead purposes and either a positive or negative E-Lead may be used to initiate ringing. The 41670 module also provides a timed "acknowledgment" output upon receipt of an incoming call along with ringback tone to the 4-wire transmit port. A ring voltage generator is also supplied.

3. SPECIFICATIONS

Power requirements	-20 VDC 50 ma idle 250 ma max. (ringing one phone)
Environmental	
Operating Temperature	0°C to 50°C
Storage Temperature	-40°C to 80°C
Relative Humidity	0% to 95% non-condensing
M-Lead and E-Lead	
M-Lead Contacts	Single Form C 1A @125VAC or 2A @ 30VDC
E-Lead Inputs	Normally open Enabled by: GND @ Pin M -12 to -24VDC @ Pin L GND @ Pin K for All Call
Voice Paths	
Transmit Level	-16 to +7 dBm @ 600Ω
Receive Level	-16 to +7 dBm @ 600Ω
Ringback Level	-20 dBm0 (nominal)
2-Wire Level	0 dBm (nominal) 600/900Ω
4-Wire Level	
MIC	0 dBm (nominal)
RCVR	-16 dBm (nominal)
Frequency Response	+1 dB, -3 dB 300 Hz to 3400 Hz (ref 1000 Hz)

4. THEORY OF OPERATION

4.1 4-WIRE PORT

4.2 Transformer T1, operational amplifier U1-A, and their associated components provide a balanced receive input on pins Y and Z. The gain of the amplifier is adjusted with potentiometer R3. When interfacing to a 4-wire Telset, U1-A drives the Telset receiver via pins P and R. When interfacing to a 2-wire telephone, U8, Q6, Q7 and associated circuitry provide a balanced output to drive the Telset receiver via pins U and V.

4.1.2. Operational amplifier U1-B is the 4-wire transmit amplifier with level adjustment provided by potentiometer R2. Transformer T2 is driven by the output of U1-B and provides a balanced output on pins H and J. Relay K2 establishes the transmit path from the Telset when off hook and allows signals to pass from the microphone of the Telset, via pins U and V, to U1-B. When the Telset is on hook, relay K1 opens the transmit path to prevent spurious signals from being transmitted.

4.1.3. An auxiliary output is available when ST-1 and ST-2 are installed. This is a single-ended output that is driven by the 4-wire receive amplifier U1-A. The auxiliary output can be used to drive other modules that do not have transformer coupled inputs for common-mode noise rejection (such as the 41632 DTMF Address Decoder).

4.2. HYBRID BALANCE CIRCUITRY

4.2.1. U1-C, U8, Q6, Q7 and their associated components comprise a balanced network to match the impedance of a 2-wire Telset. The balance network provides phase cancellation of the received signals for the transmit port, thus attenuating the signal echoed back on the 4-wire port. The network balance is adjusted by potentiometer R1.

The balanced network circuitry is not used with 4-wire Telsets.

4.3. LOOP CURRENT SUPPLY

4.3.1. U8-C, U8-D, Q6, Q7 and their associated components comprise a self balancing constant current source. This circuitry provides talk battery to the Telset for the microphone and DTMF oscillator.

4.3.2. Off hook detection is performed by Q8. If the Telset is taken off hook during ringing, increased tip current is detected by U10, which triggers U2-A to disable the ring generator. Once the ringing is disabled, Q8 will detect loop current and establish the off hook condition.

Once the off hook condition is established, relay K1 is closed via Q8 and Q2. This allows MIC signals present on the Telset to be transmitted, as well as disabling the ringing circuitry.

4.4. RING VOLTAGE GENERATOR

4.4.1. Ring cycling is provided by U2 through U6 and associated components. Transformer T3 and transistors Q4 and Q5 form a self-oscillator to generate high voltage. These are turned on by transistor Q3. The high voltage present at the secondary side of T3 is rectified by CR5-8, filtered by C31, chopped by Q10 & Q11 to produce 20Hz, and routed to the Telset by relay K2. U3 pin 13 is a 20Hz signal used to switch Q10 and Q11 via optocoupler U11 and transistor Q9 to produce the 20Hz ring signal.

4.4.2. If the Ring Voltage Generator is not included, ST-10 and ST-11 are installed for an external ring generator.

4.4.3. If a rapid ring rate is desired to identify "broadcast" calls, the "ALL CALL" output from the address decoder is connected to pin K. When an "ALL CALL" is detected, U4 gates the rapid ring rate signal to U5 and U6.

4.5. RINGBACK AND ACKNOWLEDGMENT

4.5.1. U6-D and associated circuitry generates the ring frequency which is optically coupled via U7 and summed into output amplifier U1-B. This provides a ringback which is routed to the transmit port. Ringback is disabled during ALL CALL.

4.5.2. The acknowledgement output is generated by one pole of relay K2. This output is at Logic “1” (grounded) while the Telset is ringing, and open between rings.

4.6. POWER/BIAS

4.6.1. A 12VDC regulator (U9) provides power for the digital IC's, which are powered by –20VDC and -8VDC.

4.6.2. A -10VDC bias voltage is provided to all other operational amplifiers by the output of U1-D. This operational amplifier is configured as a voltage follower.